REMARKS

OBJECTIONS

Drawings

Amendments to the drawings have been presented in response to some of the Examiner's objections to the drawings on record. No new matter has been added and support for the changes is found throughout the original specification.

The Applicant has not amended Figs. 4a, 4b, or 5b with respect to the values of the bit capacity of the lines used to re-circulate the accumulated calculation results. Although these values are not exclusive, and other embodiments may use other values, these values provide the lines with sufficient capacity to re-circulate the accumulated calculation results back to the appropriate calculation assemblies.

Similarly, the bit capacity of the lines from "Mux ~ 432" and "CRC ~ 426" of Fig. 4b; and "Mux ~ 532" and "CRC ~ 522b" of Fig. 5b are sufficient as depicted (all depicted as "32") for their respective embodiments. Again, embodiments other than the ones depicted may employ lines of different bit capacities.

The Applicant respectfully requests that the Examiner withdraw his objections to the drawings.

CLAIM REJECTIONS

35 USC 102 Rejections

35 USC 102(b) Rejections of claims 1, 2, 4, 5, and 7 based on NN901051

In the Office Action, claim 1 is rejected under 35 USC 102(b) as being anticipated by NN901051. The Applicant respectfully traverses this rejection of this claim.

Claim 1, for example, recites:

> 1. An apparatus comprising:
>
> a data word extractor to successively extract a first plurality of data word groups from a stream of input data, one data word group at a time, with each extracted data word group having a group size of at most n bytes, where n is an integer;

a plurality of CRC calculation assemblies coupled to the data word extractor to be selectively employed to incrementally calculate a CRC value for the first plurality of data word groups, the calculation being iteratively performed, one iteration at a time, and for each iteration, the selection of the CRC calculation assemblies being made in accordance with the group size of the data word group extracted for the iteration;

a plurality of storage elements correspondingly coupled to the plurality of CRC calculation assemblies to correspondingly store the results generated by the corresponding ones of the CRC calculation assemblies for one iteration of the iterative calculation; and

a plurality of selectors coupled to storage elements and the plurality of CRC calculation assemblies to selectively re-circulate one of the stored results back to the selected one of the CRC calculation assemblies for the next iteration of calculation, and to selectively output one of the stored results as the calculated CRC value at the end of the iterative calculation.

As is well established, to make a *prima facie* anticipation rejection the Examiner must provide a single prior art document that describes, either expressly or inherently, each and every element of the rejected claim. Therefore the absence of even a single limitation in the cited document constitutes an improper anticipation rejection.

NN901051 does not describe, either expressly or inherently, "a plurality of storage elements ***correspondingly coupled*** to the plurality of CRC calculation assemblies to ***correspondingly store*** the results generated by the ***corresponding ones of the CRC calculation assemblies***" as required by claim 1, for example.

The Examiner asserts that page 1 of the cited document, which states "the CRC register is composed of 16 Polarity Hold-Shift Register Latches," describes these storage elements. The Examiner goes on to state that although the drawing of Figure 1 of the cited reference doesn't explicitly show the latches that are part of each CRC generator, the "text teaches the storage latches in the above quotation (16 each) within each generator and so storage is inherent to each CRC generator."

The Applicant respectfully disagrees with this interpretation. Nowhere does the cited reference say that the shift register latches are part of each CRC **generator**. It simply states that the "CRC **Register**" depicted in Figure 1 is composed of these shift register latches. NN901051 page 1, last full sentence.

The 16 Polarity Hold –Shift Register Latches are not ***correspondingly coupled*** to the 8-bit and 16-bit CRC logic elements of the cited reference. While it is unclear how these shift register latches are arranged, it is clear that at least a portion of them are used for both the 8-bit and the 16-bit logic outputs. This is incompatible with the common understanding of the language "a plurality of storage elements correspondingly coupled to the plurality of CRC calculation assemblies." In this excerpt 'correspondingly' modifies how the storage elements and the calculation assemblies are coupled together. Specifically, the calculation assemblies are coupled to their storage element counterparts. See *Webster's Third New International Dictionary, Unabridged.* Merriam-Webster, 2002. http://unabridged.merriam-webster.com (3 May 2004) ("correspond"—to be the counterpart). If multiple calculation assemblies are coupled to the same storage elements, as they are in the cited reference, each calculation assembly is not coupled to its own storage element counterpart, as required by claim 1, for example.

This interpretation is further bolstered by the embodiment described and discussed with reference to Fig. 3 of the present application. This embodiment describes "three CRC calculation assembly and accumulator pairs **304** and **308a**, **306a** and **308b**, and **306b** and **308c** to facilitate overlapped CRC generation for two successive variable length series of data block groups." Application page 5, line 20. In this embodiment, each of the plurality of storage elements (**308a, 308b, and 308c**) are correspondingly coupled to the plurality of CRC calculation assemblies (**304**, **306a**, and **306b**, respectively) consistent with the natural reading of the claim language.

This is different from the cited reference which has two CRC logic elements (8-bit and 16-bit) sharing the same storage element (CRC register). Because the output from the 8-bit logic will be transferred through the same shift registers as the output from the 16-bit logic they will need to time-share any storage capacity of the CRC register. Among other things, this may sacrifice the ability to facilitate overlapped CRC generation for two successive variable length series of data block groups, afforded by the apparatus described in the Fig. 3 embodiment.

Furthermore, even assuming that the cited reference did describe storage elements that were correspondingly coupled to CRC calculators, which the Applicant disputes, the cited reference still does not describe "a plurality of selectors coupled to storage elements and the plurality of CRC calculation assemblies to selectively re-circulate one of the stored results back to the selected one of the CRC calculation assemblies for the next iteration of calculation, and to selectively output one of the stored results as the calculated CRC value at the end of the iterative calculation," as required by claim 1 for example.

The Examiner states that the 'plurality of selectors' are described in the cited document as "Fig. 1 'Gate 8 or 16 Data Bit CRC' block and 'CRC Register' block." The Examiner also points to the language stating that "after all has been run through the register, it may then be read..." The Applicant does not believe that these elements describe, either expressly or inherently, the above claim limitations for at least the following reasons.

The CRC Register cannot function simultaneously as the storage element and as one of the selectors of the claim. As stated above, anticipation requires a prior art reference that describes, either expressly or inherently, each and every element of the claim. Additionally, the elements of the reference need to be "arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F. 2d 1542 (Fed. Cir. 1983)). Claim 1, for example, recites "a plurality of selectors coupled to storage elements." The selectors and storage elements are distinct elements coupled to one another as stated. Therefore Examiner's assertion that the CRC register both selects and stores does not sufficiently describe elements of the cited reference corresponding to the elements of the claim, as arranged in the claim.

Additionally, neither of the purported selectors of the cited reference selectively outputs one of the stored results as the calculated CRC value at the end of the iterative calculation. The Examiner asserts that the Gate and the CRC Register are the selectors, however, neither of these selectively output one of the stored results. Referring again to the portion of the cited reference to which the Examiner quotes, i.e.,

"after ***all*** the data has been run through the register, it may then be read by the microcode and appended to the data stream." *NN901051* page 2, 4th sentence. The register passively stores the FCS and the microcode extracts the data from the register and appends it to the frame it wants to send. NN901051 page 3, 2nd sentence. Therefore, the 'selectors' of the cited article simply store the results without selectively outputting them as required by claim 1, for example.

Moreover, the cited reference does not have a plurality of selectors to selectively re-circulate...and to selectively output..." results. Even assuming that the apparatus of the cited reference selectively re-circulates and selectively outputs results, which the Applicant disputes, the cited reference still does not describe "***a plurality of selectors***" that do these functions as required by claim 1, for example. The 'Gate 8 or 16 Data Bit CRC' block, which the Examiner describes as one of the selectors, is not used to either selectively re-circulate or to selectively output results. This element gates the output of the logic so that the proper result is gated to the register. *NN901051* page 2, 3rd sentence. It does not "selectively re-circulate one of the stored results back to the selected one of the CRC calculation assemblies for the next iteration of calculation" as required by claim 1, for example. Nor does the gate element selectively output one of the results.

Therefore, because these elements are not found in the cited document, a 35 USC 102 rejection is improper. Of course, there are other bases on which claim 1 may be distinguished from the cited reference and Applicant does not rely solely on the distinction above; however, this is believed to be more than sufficient to overcome this rejection. Therefore, it is respectfully requested that the Examiner's rejection of claim 1 be withdrawn.

Furthermore, claims 2, 4, 5, and 7 are dependent upon, and incorporate the same limitations as, claim 1. Thus, for at least the same reasons these claims are patentable over NN901051. The Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

35 USC 102(b) Rejection of Claims 12, 13, 15, 16, and 18 based on NN901051

In the Office Action claim 12 is rejected under 35 USC 102(b) as being anticipated by NN901051. The Applicant respectfully traverses this rejection of these claims.

Claim 12, for example, recites:

> 12. A method comprising:
>
> successively extracting a first plurality of data word groups from a stream of input data, one data word group at a time, with each extracted data word group having a group size of at most n bytes, where n is an integer;
>
> selectively employing a plurality of CRC calculation assemblies coupled to the data word extractor to incrementally calculate a CRC value for the first plurality of data word groups, with the calculation being iteratively performed, one iteration at a time, and for each iteration, selecting the CRC calculation assemblies in accordance with the group size of the data word group extracted for the iteration;
>
> correspondingly storing the results generated by the plurality of CRC calculation assemblies for one iteration of the iterative calculation into a plurality of storage elements; and
>
> selectively re-circulating one of the stored results back to the selected one of the CRC calculation assemblies for the next iteration of calculation, and selectively outputting one of the stored results as the calculated CRC value at the end of the iterative calculation.

NN901051 does not describe, either expressly or inherently, "correspondingly storing the results generated by a plurality of CRC calculation assemblies for one iteration of the iterative calculation into a plurality of storage elements" as required by claim 12, for example.

As previously mentioned the shift registers of the CRC register are not correspondingly coupled to the CRC logic assemblies. Furthermore, the CRC register does not correspondingly store the results generated by the CRC logic assemblies into a plurality of storage elements. Because the CRC logic assemblies share the storage functionality of the CRC register, they must alternatively store their respective outputs there.

Of course, there are other bases on which claim 12 may be distinguished from the cited reference and Applicant does not rely solely on the distinction above; however, this is believed to be more than sufficient to overcome this rejection. It is respectfully requested that the Examiner's rejection of claim 12 be withdrawn.

Claims 13, 15, 16, and 18 are dependent upon, and incorporate the same limitations as, claim 12. Thus, for at least the same reasons these claims are patentable over NN901051. The Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

35 USC 103 Rejections

35 USC 103 Rejection of claim 10 based on NN901051 in view of Albertango

The Examiner has rejected claim 10 based on NN901051 in view of Albertango. The Applicant respectfully traverses this rejection of this claim.

As discussed above, NN901051 does not describe, either expressly or inherently, "a plurality of storage elements ***correspondingly coupled*** to the plurality of CRC calculation assemblies to ***correspondingly store*** the results generated by the ***corresponding ones of the CRC calculation assemblies***" as required by claim 1, for example. Claim 10, is dependent upon and includes the same limitations as claim 1. And because Albertango does not correct for these deficiencies, claim 10 is patentable for at least the same reasons. The Applicant respectfully requests that the Examiner withdraw his rejection of this claim.

35 USC 103 Rejection of claims 20, 21, 23, 24, and 26 based on NN901051 in view of Albertango

In the Office Action claim 20 is rejected under 35 USC 103(a) as being unpatentable over NN901051 in view of Albertango. The Applicant respectfully traverses this rejection of this claim.

Claim 20, for example, recites:

20. An apparatus comprising:

a plurality of processing units to correspondingly process a plurality of network traffic flows; and

a shared CRC generation block coupled to the processing units to alternately generate a CRC value for a data block of a selected one of the network traffic flows, the shared CRC generation block including at least one CRC generation unit to iteratively generate a first CRC value for the data block of the selected one of the network traffic flows, the at least one CRC generation unit including a plurality of CRC calculation assemblies to be selectively employed to incrementally calculate a CRC value for a first plurality of data word groups, the calculation being iteratively performed, one iteration at a time, and the selection of the CRC calculation assemblies for the various iterations being made in accordance with group sizes of extracted data word groups of the first plurality data words for the various iterations.

Neither NN901051 nor Albertango, alone or in combination, suggest, teach or discuss "a plurality of processing units to correspondingly process a plurality of network traffic flows," as required by claim 20, for example.

The Examiner concedes that NN901051 "does not specify a plurality of processor units for processing network traffic," but goes on to say that Albertengo "does teach combining a CRC generator in line with the data flow (page 70 column 1 last 2 paragraphs) in an analogous router (page 70 column 2, paragraph 3), as claimed by the Applicant. Even if this were an accurate interpretation, it still does not provide the above mentioned limitations from claim 20, for example.

The language of Albertango that the Examiner refers to relates to cyclical codes for block-transfer oriented buses. More specifically, "[w]hen ***a block of data*** transfers on the bus, every module involved in the transaction calculates the parity-check word by means of its own parallel CRC generator." Albertango page 70, column 1, last paragraph.

In the cited reference, a block of data transfers to the local bus, is processed by different bus module circuits on the local bus, and the parity-check word is generated for that data block. After the CRC is done with the data words of the data block, a "calculated check word is written on the bus and can be read just as if it were an

additional data word." Albertango page 70, column 2, 1st paragraph. This is not the same as a plurality of processing units to ***correspondingly process a plurality*** of network traffic flows," as required by claim 20, for example. It is simply one network traffic flow (one data block) that may be incrementally processed through a plurality of bus modules. At most, the cited reference teaches a plurality of processing units to ***sequentially process*** a plurality of network traffic flows.

Because the cited references fail to describe the above claim limitation, the examiner has not made a *prima facie* case that in view of the cited references, the claimed invention "as a whole" would have been obvious at a time before the invention was made to a person skilled in the art, as required for an obviousness rejection. The Applicant respectfully requests that the Examiner withdraw this rejection of this claim.

The Examiner has also rejected 21, 23, 24, and 26 under 35 USC 103(a) as being unpatentable over NN901051 in view of Albertango. Because these claims depend upon, and include the same limitations as claim 20, they are patentable for at least the same reasons. The Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

35 USC 103(a) Rejection of Claim 11 based on NN901051 in view of Shih

The Examiner has also rejected claim 11 under 35 USC 103 as being unpatentable over NN901051 in view of Shih. This rejection by the Examiner of this claim is respectfully traversed.

As discussed above, NN901051 does not describe, either expressly or inherently, "a plurality of storage elements ***correspondingly coupled*** to the plurality of CRC calculation assemblies to ***correspondingly store*** the results generated by the ***corresponding ones of the CRC calculation assemblies***" as required by claim 1, for example. Claim 11 depends upon and includes the same limitations as claim 1. And because Shih does not correct these deficiencies, claim 11 is patentable for at least the same reasons. Therefore, the Applicant respectfully requests the Examiner to withdraw his rejection of this claim.

CONCLUSION AND EPILOGUE

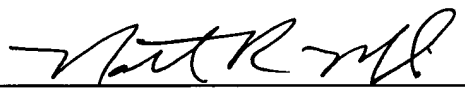
In view of the foregoing, the Applicant respectfully submits that claims 1-27 as presented are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2972.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 5/5/04



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